NTU Journal for Renewable Energy (2024) Vol. 6 (1): 21-30
DOI: https://doi.org/10.56286/ntujre.v6i1

IRAQI Academic Scientific Journals

EISSN: 2788-9920
NTU Journal for Renewable Energy
Available online at:
https://journals.ntu.edu.iq/index.php/NTU-JRE

Analysis of the performance of a 25-level inverter with a minimum number of switches and reduced harmonics for an environment solar energy

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Article Information

Received: 13 – 02 - 2024
Accepted: 01 – 03 - 2024
Published: 03 – 03 - 2024

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Key words:
PV solar; Maximum Power Point Tracking (MPPT); Multilevel inverters (MLI); MC-SPWM algorithm; Total Harmonic Distortion (THD).

ABSTRACT

A multilevel inverter is a type of electrical equipment that converts a DC voltage to a higher AC value by creating a stepped waveform using several voltage levels. Multilevel inverters may create waveforms with three or more voltage levels, although regular inverters cannot. This separation results in lower harmonic distortion, decreased electromagnetic interference, and higher efficiency. An innovative MLI design that makes use of fewer switches and PV sources solves this problem. The Perturbation and Observation (P&O) approach is used to derive the Maximum Power Point Tracking (MPPT) from these PVs. The MC-SPWM technique was used in the design, simulation, and construction of single-phase and three-phase multilevel inverters with inverter levels ranging from three to twenty-five. The technique's cornerstones are phase disposition (PD-PWM) and power quality improvement. The main goal of the paper objectively analyzing the issue of power-system harmonics, providing information on causes, effects, and useful harmonic mitigation strategy.

1. Introduction

These days, there is a lot of interest in renewable energy sources. as a result of the availability of reserves and the lack of pollution. As a result, public opinion is generally in favor of using renewable energy. A form of converter called a multilevel inverter can provide the right level of alternating voltage at the output by using dc voltages as inputs. Systems that use renewable energy have been the main applications for multilayer inverters. Unconventional energy systems are using multilevel inverters more frequently due to their improved performance, reduced dv/dt stress power electronics switches, and creative switching topologies [1],[2]. PV systems discovered that the multilevel inverter produced waveforms with fewer harmonics and of higher quality. To attain high reliability and efficiency, researchers have developed a variety of inverters with various topologies. These inverters are useful for applications requiring medium to high power. Multilevel inverters are the best choice for solar systems to achieve peak efficiency in the production of renewable energy. The suggested setup is a cascade system with sinusoidal PWM control. The PV system usually employs an inverter and a boost converter to supply the utility with AC power [3]. Power semiconductor switches make it possible for the converter/inverter to operate as needed. The tracking algorithm modifies the converter's duty cycle for each given irradiance/insolation to guarantee that the PV cell output voltage matches the voltage corresponding to the maximum point. A PV system that uses an inverter or converter exposes the utility to harmonics and lowers the quality of the power it produces. Numerous modulation methods, including space vector modulation (SVM), fundamental frequency switching, selective harmonic elimination (SHE-PWM), sinusoidal pulse width modulation (SPWM), and others, have been refined for use with multilevel inverters [4]–[6].

1.1 Literature Review

In 2018 [7], A 27-level cascading inverter with single and three phases and input voltages of 1 Vdc, 3 Vdc, and 9 Vdc was simulated using MATLAB. The enhanced absolute sinusoidal pulse width modulation (ASPWM) technique was used in conjunction with an inductive load. The THD values of the single-phase circuit were 0.238% and 1.165% with the same current and voltage, whereas the three-phase circuit had THD values of 0.67% and 0.0857%, respectively. In 2019 [8], The decision was made to use low-power electrical devices and DC voltage sources to create a 13-level inverter. The output voltage THD was 9.5% when using a zero-level (ZL) inverter and 12.5% when not using a zero-level. (NZL) inverter.

In 2020 [9], presented a brand-new 25-level asymmetric multilevel inverter architecture basic unit. In order to increase the output voltage level, the extended and cascaded topologies were developed. Furthermore, two methods for figuring out each unit's DC source values' magnitude are explained. Using a lab setup for 25-level output and the MATLAB/Simulink tool, the performance of the recommended topology is verified. Using various loading conditions, the dynamic performance of the proposed topology is verified; the output's THD value was 3.62%.

In 2021[10], created a multilevel inverter architecture with 25 stages for use in high power applications. Rather of using dc sources to satisfy loads, the suggested paradigm uses twelve different PV arrays. For output, a cascade setup is used. It operates by PWM control. MATLAB/Simulink is used to simulate the recommended model's implementation. The results indicate a THD of 3.36%. The suggested model includes 48 IGBTs, 48 freestanding PV arrays, and 12 hybrid bridges with four switches per to meet load requirements.

In 2023 [11], recommended investigating three H-bridge asymmetric DC sources in an MLI. With two control techniques, LS-SPWM and PS-SPWM, the suggested inverter is made into a multilayer inverter with reduced THD and fewer switching components. The investigation's conclusions indicate that, depending on the kind of loads used in the circuit's testing—resistive or inductive—the voltage's THD decreased by 1.28%. The THD of the current decreased by 1.28% and 1.25% for resistive and inductive loads, respectively.

2. Photovoltaic Theory

2.1 Solar Energy

Solar energy is the globally most accessible renewable energy source [12]. The unlimited supply and environmental friendliness of the photovoltaic (PV) system are the reasons why it is becoming more and more popular. PV systems have a long lifetime with a little maintenance. Solar radiation and temperature can affect PV systems since they depend so much on certain atmospheric conditions. PV cells transform radiation energy into electrical energy. There is only one maximum power point (MPP) and tracking this point is very important, so that methods that used to track this point called MPP tracking (MPPT) techniques [13, 14].

2.2 The Perturb-and-Observe (P&O) Technique

The flowchart of this method is illustrated in figure (1). Because of its ease of use and simplicity, and cheap processing power requirements, the (P&O) technic is one of the most commonly utilized MPPT algorithms. The method requires regulating the duty cycle of the DC-DC converter to regulate the operating voltage of the DC connection between the PV array and the DC/DC converter. The fundamental disadvantage of the P&O MPP approach is oscillating about the MPP rather than monitors it directly. Since the operating point does not stop perturbing in both directions when it gets very close to the MPP, it does not stop at the MPP point. By reducing the perturbation step size, the oscillation can be reduced [15].

2.3 Maximum Power Point Tracking (MPPT)

Recent developments have a major influence on solar energy's capacity to fulfill the world's expanding energy demand. The high initial cost of PV components is making it harder to build and maintain PV systems. The low conversion efficiency of PV modules is another barrier preventing the expansion of PV systems. To optimize energy harvesting from current environmental conditions, research is concentrating on the integration of MPPT-capable power converters into PV systems [13]. Operating at sites distant from the MPP might result in significant power losses due to the MPP being unstable due to temperature and irradiance fluctuations in the weather. To ensure that the PV panels generate the most electricity possible under all circumstances, the MPP has to be monitored. Keep in mind that the PV settings and the weather have an impact on this [14]. PV systems need to be more productive. In this study Perturb and Observe (P&O) algorithm is used to track the MPP due to its simplicity and ease of implementation as shown in figure (2). While figure (3) depicts the boost converter's circuit diagram. A boost converter is designed by choosing components and calculating their values depending on the required output voltage and current.

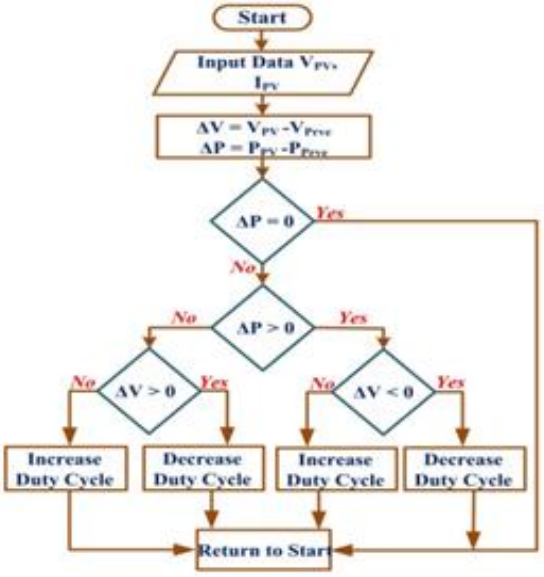


Figure 1. Flow Chart of the P&O technique.

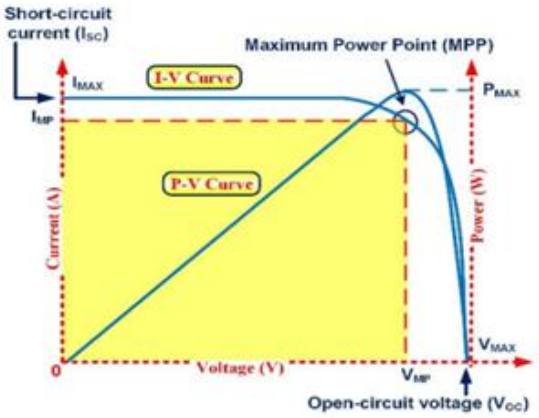


Figure 2. Mechanism of P&O algorithm.

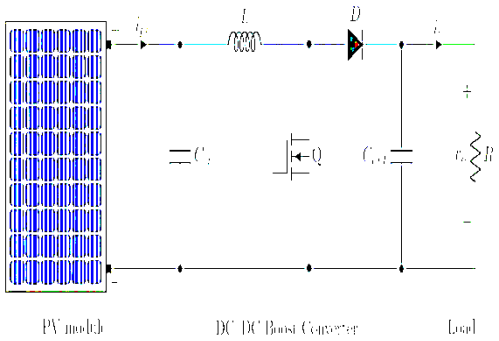


Figure 3. DC-DC Boost converter circuit.

The duty cycle (D) of the boost converter, the minimum boost inductor (L), and the output capacitor (C_{out}) of this converter are determined as [16]:

$$D = 1 - \frac{V_{in}}{V_{out}} \quad (1)$$

$$L = \frac{Vo\,(1-D)}{\Delta I_L f} \quad (2)$$

$$C = \frac{(1-D)}{8L\left(\frac{\Delta Vo}{Vo}\right)f2} \quad (3)$$

Where $\left(\frac{\Delta Vo}{Vo}\right)$ is the outputs voltage ripple and calculated at 3%, (R) is output resistance, and (f) is the switching frequency [55]. The values of L=1mH, C_{out}=2mF.

2.4. Modelling of a PV Module

The most basic part of a solar panel is the solar cell. A module is composed of many low-voltage photovoltaic cells coupled in parallel to generate a high current and in series to generate a high voltage [17]. Despite the fact that solar panels are composed of many modules, the terms "solar module" and "solar panel" are frequently used interchangeably. The photovoltaic cells, grouped in panels and arrays, transform solar radiation into electrical power. Each cell functions as a diode in the presence of sunlight, generating pairs of electron-hole pairs. The diode's p-n junction generates an electric field that causes the electrons and holes to travel, and the junction potential drives these particles to an external circuit [18]. Some heat losses are brought on by the cell's shunt resistance and current leakage at the p-n junction. The analogous circuit of a PV cell is shown in Figure (4). A PV cell's output current may be computed as follows: -

$$I_{out} = I_p - Ir_{st} \times \left(e^{\frac{Vout + Iout \times Rs}{Dcf * Vch}} - 1\right) - \frac{Vout + Iout \times Rs}{Rsh} \quad (4)$$

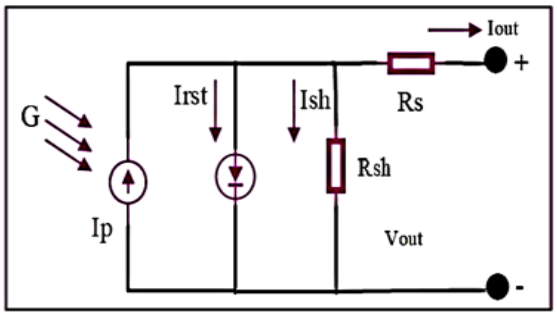


Figure 4. PV Cell's Equivalence Circuit.

where Ip is the photocurrent, Irst is the reverse saturation current of the matching diode, R_{sh} is the shunt resistance, and R_S is the series resistance. A perfect photovoltaic cell has $R_{sh} = \infty$ (ground leakage) and $Rs = 0$ (loss of series). PV conversion efficiency is neither influenced or indifferent to changes in R_{sh}, while it is sensitive to little fluctuations in Rs. A slight increase of Vg might result in a significant decrease in PV production. Equation [19] states that the temperature-dependent thermal voltage, or V_{th}, is determined by the quality factor of a diode, or DcF.

$$Vth = \frac{K \times T}{q} \quad (5)$$

Where K is constant Boltzmann and equal to 1.308610−23 J/K, T is the working temperature, q is the electron charge and equal to 1.308610−191.602210 C.
Consequently, the voltage value is mostly determined by the working temperature. One may compute the photocurrent I_p using [20]:

$$I_p = \frac{GT}{GT,ref} \times [Ip,rfe + \mu Isc \times (Ta,ref)] \quad (6)$$

Where $G_{T,ref}$ is the reference irradiance, G_T is the actual irradiance, $T_{a,ref}$ is reference temperature, T_a is the actual temperature, and μ_{Isc} is the temperature coefficient for short circuit current.
The reverse saturation current, I_{rst}, is calculated as follows:

$$I_{rst} = I_{rst,ref} \times \left(\frac{Ta}{Ta,ref}\right)^3 \times e^{\frac{-q\Theta}{DcFk}\left(\frac{1}{TC} - \frac{1}{TC,ref}\right)} \quad (7)$$

where θ is the energy of the band gap. Since manufacturers do not give the values of the shunt and series resistances, it is difficult to determine the precise values of the parameters in the preceding calculations. However, several well-established methods exist for estimating these values, such as the Newton-Raphson approach, which requires an accurate evaluation of the initial values for calculations [21]. The voltage generated by renewable energy sources changes over time, however in order to transform the erratic DC voltage level to a constant DC voltage level, a converter and regulator are essential. The PV parameters are explained in Table 1.

Table 1. The PV panel specifications.

Components	Symbols	Value
1Soltech 1STH-215-P	PV1&PV2	1 Series x 1 parallel
	PV3&PV4	5 Series x 3 parallel
Maximum power	P_{Max}	213.15W
Open Circuit Voltage	Voc	36.3V
Short –Circuit Current	Isc	7.84A
Voltage at maximum power point	Vmp	29V
Current at maximum power point	Imp	7.35A
Input Capacitor	C_{PV}	1mF

3. The Multilevel Inverter Methodology

In recent times, industrial medium-voltage applications have highly focused on Multilevel Inverters (MLI) [22]. While working with medium voltage grids, the MLI has shown to be the most advantageous choice because of the restrictions of 2-Level inverters with regard to semiconductor blockage voltage in this range. In order to comply with grid rules, the MLI lowers the voltage's total harmonic distortion (THD) and the stress of voltage differential over time via semiconductor switches. Moreover, it has been demonstrated that they can produce semiconductor switches with lower power dissipation and electromagnetic interference (EMI) [23]–[26]. Based on its architecture, MLIs are often classified into three fundamental topologies: Cascaded H-Bridge (CHB), Flying Capacitor (FC), and Neutral Point Clamped (NPC) [27]. Because of its versatility and easy modification to several levels, the CHB is widely used. It is built in a modular manner. Because there are more driving circuits and components in standard multilevel inverters, As the number of levels increases, the design and control circuits get increasingly complex. In addition, the reliability of the system decreases with the number of discrete components. In order to improve the output voltage waveform and increase component utilization, new multilayer inverter topologies have been designed lately [28]. Current studies on this type of inverter focus on two main areas: first, creating topologies that power electronic switches with fewer dc link sources; second, creating techniques for altering triggering angles to lessen harmonics produced while the inverter is operating. [29]–[32].

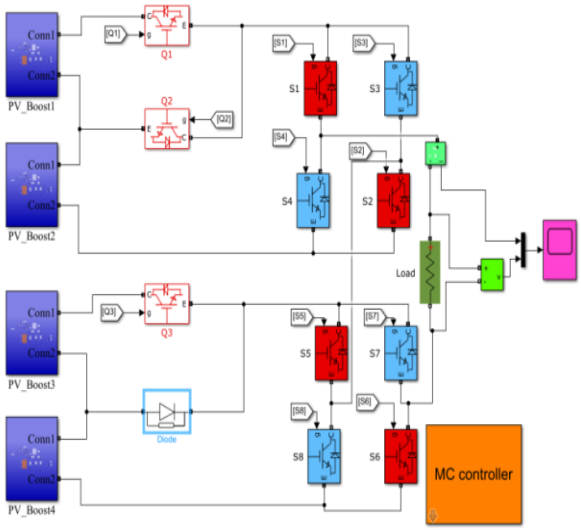


Figure 5. The proposed 25-level inverter circuit with PVs sources.

3.1 The 25-level inverter proposed

A 25-level output voltage is produced by the suggested. The suggested design has fewer switches than the preceding kinds, with just 11 switches, 1 diode, and an overall DC voltage source configuration of (1:1:5:5) Vdc. This characteristic, which lowers switching losses as well as total costs in electronic circuits, is crucial, particularly when dealing with three-phase circuit connections. Figure (5) illustrates the suggested 25-level inverter circuit. The switching patterns needed to produce an output voltage with 25 levels are presented in Table (2). The benefit of this suggestion is that there are fewer switches—just the positive portion's patterns are specified. To obtain the negative part's patterns, we reverse the states of switches S1 through S8 in the positive part. Figure (6) displays the current route

diagram in various operating modes at varying levels, based on the switching scenarios mentioned in Table (2). This work proposes an asymmetric MLI topology to address some of the issues with conventional cascaded MLIs. The suggested MLI structure takes advantage of the staircase modulation technique, which raises output voltage levels with fewer switches or active devices. By contrasting the obtained findings with the existing standard cascaded H-bridge MLIs, the results are confirmed.

Table 2. Switches states of the 25-level output voltage.

Conducting switches: 1 =ON; 0= OFF											
Q 1	**Q 2**	**Q 3**	**S 1**	**S 2**	**S 3**	**S 4**	**S 5**	**S 6**	**S 7**	**S 8**	**V_{out}**
1	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**15Vdc**
0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**14Vdc**
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**13Vdc**
0	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**12 V_{dc}**
1	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**11 V_{dc}**
1	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**10 V_{dc}**
0	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**9 V_{dc}**
0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**8 V_{dc}**
0	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**7 V_{dc}**
1	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**6 V_{dc}**
1	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**5 V_{dc}**
0	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**4 V_{dc}**
0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**3 V_{dc}**
1	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**2 V_{dc}**
0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1 V_{dc}**
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0 V_{dc}**

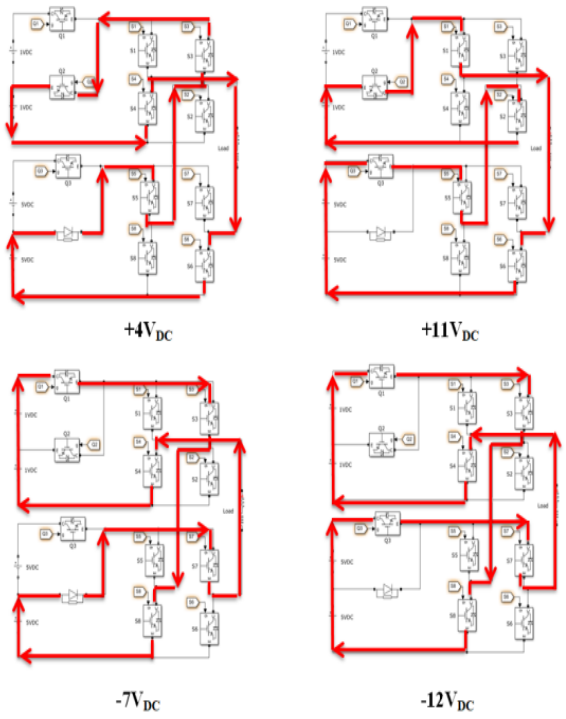


Figure 6. The current path diagram in some operating modes at different levels of the 25-level.

3.2 Multi Carrier Sinusoidal PWM (MC-PWM) Technical

Multi carrier SPWM, which is derived from different power switching inverters, is one of the most used PWM approaches. The SPWM produces gate signals for the inverter switch by comparing the source voltage's sine wave to a triangular carrier wave. One may consider energy waste to be a significant issue for high-power applications. By using a simple SPWM frequency control technique, switching losses may be decreased [33].Level-shifted modulation (Carrier Disposition (CD) PWM) techniques may be classified into three types: phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). Carriers above and below the reference point have a phase opposition disposition (POD) that is 180 degrees out of phase. APOD stands for alternative phase opposition disposition, which phases-shifts the carriers of adjacent bands by 180 degrees. Every carrier in every band is in phase when it comes to the phase disposition (PD). This technique offers the lowest harmonic at greater modulation indices in contrast to the other disposition techniques. Though it

results in an uneven device state, level-shifted multicarrier modulation offers superior harmonic attenuation [34], [35]. Figure (7) shows how a sine wave reference is used in conjunction with multicarrier PWM to produce a 25-level output voltage.

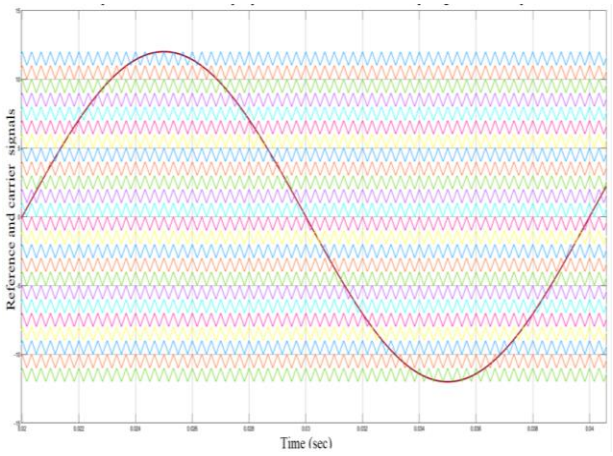


Figure 7. MC-PWM algorithm using PD technique.

4. Results and Discussion

This section involves modeling a single-phase 11-switch without an LC filter using MATLAB/SIMULINK and one diode. Our multilevel inverter is tested with a light inductive load of (R = 100Ω, L = 50 mH) and a switching frequency of 3 kHz to evaluate its performance. Our goals are to offer a sinusoidal voltage with maximum efficiency, minimum switching loss, enhanced harmonic characteristics (THD), and frequency and amplitude set by the reference signal at the lowest feasible cost. A 25-level single-phase inverter with a PV array was simulated using MATLAB/Simulink, as shown in Figure (5). The single-phase current and voltage waveform in Figure (8) contains 25 levels of level change at levels ranging from 3 to 25 levels. Figure (9), on the other hand, displays the output voltage and current waveforms together with an FFT analysis of the (1ϕ 25-L) It is note that the resulting voltage is equal to (311V), while the voltage shown in the drawing is equal to (11.96 V), meaning that it is multiplied by a gain during design equal to (1/26). This system is built as a three-phase system and Figure (10) shows the 3ϕ voltages and currents of the 25-level with their FFT analysis. while Figure (11) shows the THD of the 25-level output voltages with respect to voltage levels for single-phase and three-phase respectively.

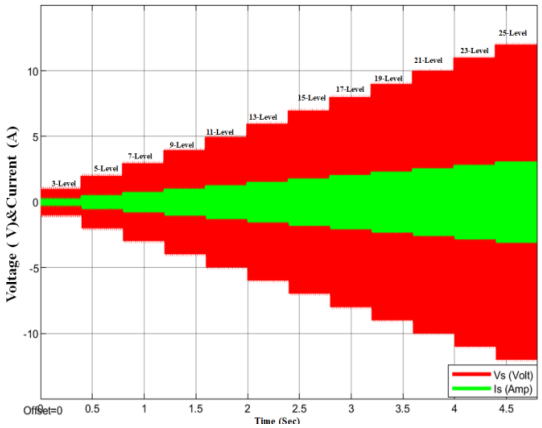
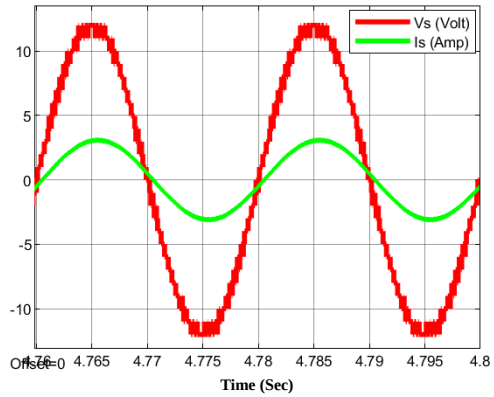
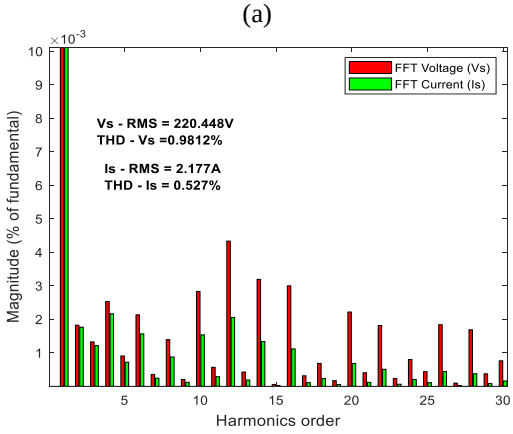


Figure 8. Output voltage of the (1ϕ 25-L) change at levels ranging from 3 to 25 levels.

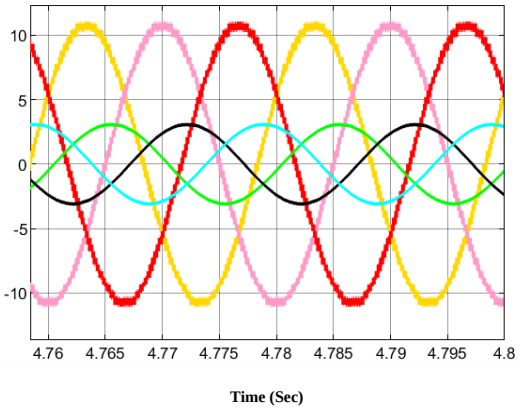


(a)

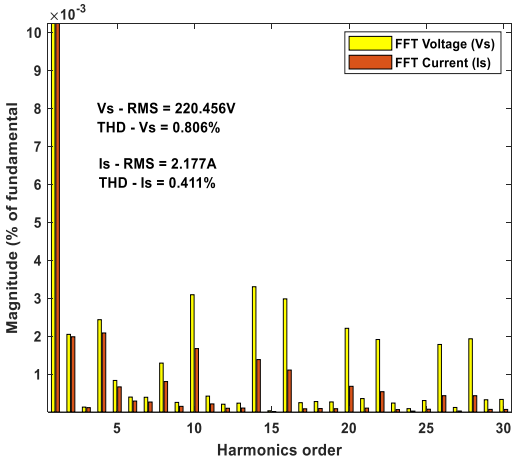


(b)

Figure 9. (a)The output voltage and current waveforms with their (b) FFT analysis of the single phase 25-level inverter.

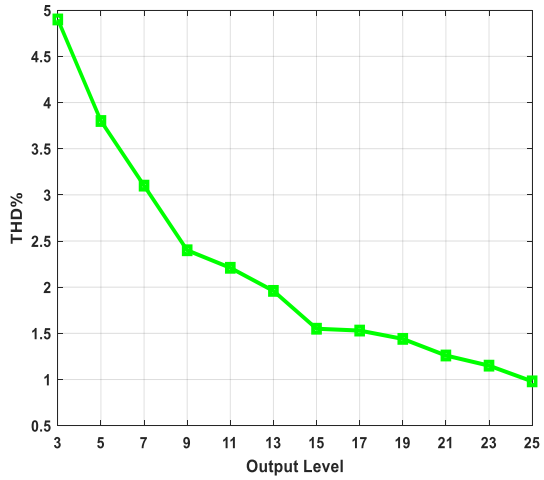


(a)

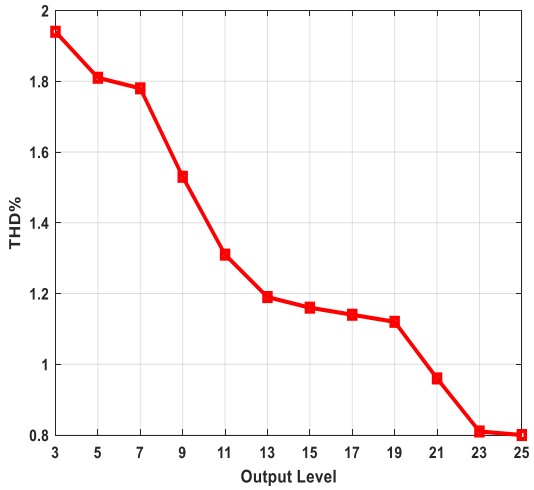


(b)

Figure 10. (a)The output voltage and current waveforms with their (b) FFT analysis of the three-phase 25-level inverter.



(a)



(b)

Figure.11 THD of the output voltages with respect to voltage levels (a) (1ϕ 25-L) , (b) (3ϕ 25-L).

To highlight the benefits and characteristics of the suggested 11Sw-25L Voltage Inverter, it is crucial to contrast it with other comparable designs. With just 11 active switches, the suggested multilevel inverter can synthesize 25 levels at the output terminals. In contrast, conventional topologies require up to 48 active switches in addition to other components. Table (3) provides a summary of how this 25-level inverter compares to alternative topologies.

Table 3. Comparing between our proposed 1ϕ with conventional topologies of system volume.

	11Sw-25L	25L-CHB	25L-NPC	25L-FC	25-MMC
Actives switches	11	48	48	48	48
DC sources	4	12	24	24	24
THD-V (%)	0.98	9.8	_	_	_
Clamped diodes	1	0	552	0	0
Flying capacitors	0	0	0	276	24

5.Conclusions

This research focuses on the multi-carrier-PWM modulation approach for activating the power switches and managing the output voltage levels. A novel multilevel inverter architecture that requires the fewest power electronic components is presented in

this study. This study proposes an improved multilevel 25-level inverter that requires just 11 switches, a significantly small amount compared to traditional multilevel inverters. It is discovered that the utility voltage's harmonic content satisfies IEEE-519 standards and THD-V is around 0.98% in single phase and 0.88% in three phase and THD-I equal 0.52% in single phase and 0.41% in three phases. The benefits and validity of the suggested topology and modulation technique are shown by the simulation results. As a result, the suggested 25-Level inverter is a good and enhanced option for grid-tie PV system applications.

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