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Design and Analysis of seven multilevel Cascaded H-Bridge inverter controlled by FPGA

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A B S T R A C T

This research focuses on the design and analysis of a seven multilevel cascaded H-Bridge CHB inverter system, with particular emphasis on its control mechanism implemented using Field-Programmable Gate Array (FPGA) behavioral modeling, very high speed integrated circuit hardware description language (VHDL) code, which is created and verified with the Xilinx Integrated Synthesis Environment ISE 14.7 software. The proposed system employs seven cascaded H-Bridge inverters to achieve higher voltage levels and better waveform with lower Total Harmonic Distortion (THD) compared to traditional inverters. To demonstrate this concept, the entire system has been examined and simulated using the MATLAB/Simulink software package. Different values of THDs, Vrms and voltage waveforms have been achieved. The experimental values were compared with that achieved in simulation, and the comparison proved that the results meet the expectations.

Introduction

Due to their many benefits, including low common mode voltage, less voltage stress on power semiconductors, less dv/dt ratio when compared to two-level topologies, in addition to that low THD [1], MLIs have drawn a lot of attention in applications involving medium-voltage and high-power ranges [2], The working principle of MLIs is to generate a staircase voltage waveform similar to sinusoidal waveform with high power quality [3]. The significant advantages of MLI that's its able to decrease the voltage stress on all power devices due to the use of multilevel on the DC bus, improve the performance of the output voltage, and reduce THD [4] .The THD is an indication of harmonic pollution in the power system and it is noticed that any variations in both DC voltages and the inverter switching angles affect the output voltage THD. It can be defined as ratio between the summation of all harmonic components and the voltage or current fundamental component [5].

There are many different configurations for MLI, such as cascading H-bridge CHB, flying capacitors FC, and Neutral Point Clamped NPC MLIs [6].as shown in Fig.1[7].The first two types are using diodes and capacitors while in the CHB doesn't. The most often used is the CHB MLI, sometimes referred to as the multi-cell converter topology, because of its modular design , simplicity in control and each H-bridge has the same identical configuration and can extremely reduce a large quantity of bulky transformers that are needed by the conventional multi pulse inverters [8]. Also it needs less components in comparison to the NPC and the FC Inverters [9]. This make it more preferable for power quality and transmission system applications [10]. CHB are widely used due to benefits such as lower switching losses, the ability to achieve the same number of voltage levels with a very small number of components, and the output waveform of THD is low without the use of a filter circuit [11]. However, it has limitations such as the use of separate DC sources, which limits its applications [12].The advantages and disadvantages of each type of the Multilevel Inverter is listed in Table 1.

TABLE 1. Advantage and Disadvantage of Multilevel Inverter types

Topology	Advantage	Disadvantage
Diode Clamped	1.Simple structure. 2.At high levels THD is low. 3.High efficiency. 4.Simple control. 5.Single DC source.	1.Unequal conducting duty. 2.Un even loss distribution. 3. Capacitor's voltage Unbalanced. 4 .High voltage rating for blocking diodes.
Flying Capacitor	1.High efficiency at high voltage levels. 2. Capacitors voltage levels are Balanced . 3. Single DC source.	1. large no. of capacitors. 2.Unequal conducting duty. 3.Very complicated to control.
Cascaded H-Bridge	1.Reduce the Voltage stress on power switches. 2. Eliminate Filters. 3.High Modularity. 4.Redundancy and fault tolerant capacity. 5.Many DC sources.	1.It may be limited in some applications because it depending on separated DC source.

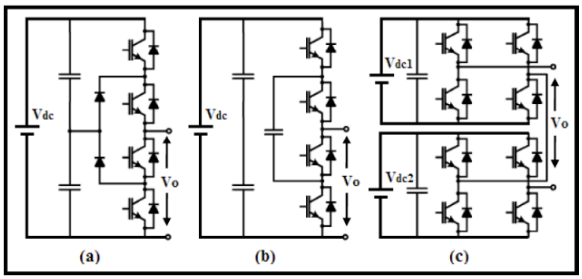


Figure 1. MLI Topologies: (a) NPC, (b) FC, (c) Cascaded H-Bridge Inverter

1. Operation Principle of a Cascaded H-Bridge Inverter

The cascaded H-bridge MLI structure formed by connecting single phase H-bridge inverters in series with independent DC sources, such as battery, fuel, or solar cells. The output obtained voltage is equal to the sum of the generated voltage from each cell [13].

$$Vo(\omega t) = Vo1(\omega t) + Vo2(\omega t) + VoN(\omega t) \quad \text{..... (1)}$$

The topology of the Cascaded H-Bridge is shown in Fig.2 [2]. The Switching states of the twelve power switches for seven level cascaded H-bridge MLI twelve power switches are displayed in Table 2.

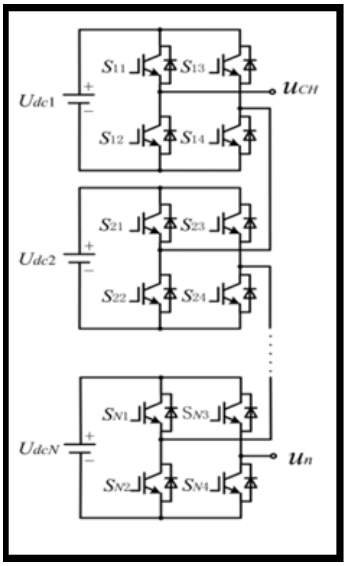


Figure 2. Structure of Cascaded H-bridge Inverter

TABLE 2. Switching Pattern of seven level Cascaded H-bridge Multilevel Inverter

Vdc	S11	S14	S13	S14	S21	S24	S22	S23	S31	S34	S33	S32
+3	1	1	0	0	1	1	0	0	1	1	0	0
+2	1	1	0	0	1	1	0	0	0	1	0	1
+1	1	1	0	0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0	1	0	1
	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	1	0	1	0	1	0	1	0
-2	0	0	1	1	0	0	1	1	1	0	1	0
-3	0	0	1	1	0	0	1	1	0	0	1	1

The output voltage level equals to 2N+1, where N: represent the number of DC sources, the below Fig.3 shows a seven-level output voltage of the cascaded H-bridge Inverter [13].

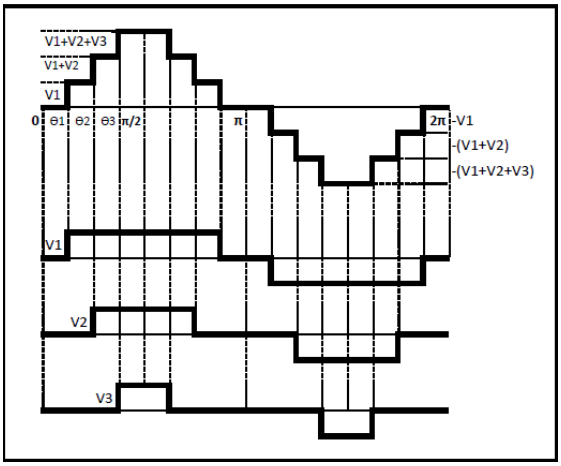


Figure 3. Seven-level cascaded multilevel inverter waveform

1.1 Fourier series Analysis for MLI

The Fourier series equation of the output voltage waveform (Vo(ωt)) of Fig.3 can be explained as below [13]:

$$Vo(wt) = \frac{Ao}{2} + \sum_{n=1,2,3}^{\infty}(A_n \cos \text{nwt} + B_n \sin \text{nwt}) \quad (2)$$

And according to Fig.3 the switching angles must follow the below conditions:

$$\theta 1 < \theta 2 < \theta\, 3 < \frac{\pi}{2}$$

After some derivations, the final equations can be expressed as follows:

$$\frac{4Vdc}{\pi}(\cos \theta 1 + \cos \theta 2 + \cos \theta 3) = H1 \quad \text{...(3)}$$

$$\frac{4Vdc}{3\pi}(\cos 3\,\theta 1 + \cos 3\,\theta 2 + \cos 3\theta 3) = H3 \quad \text{...(4)}$$

$$\frac{4Vdc}{5\pi}(\cos 5\,\theta 1 + \cos 5\,\theta 2 + \cos 5\theta 3) = H5 \quad \text{...(5)}$$

$$\frac{4Vdc}{n\pi}(\cos n\,\theta 1 + \cos n\,\theta 2 + \cos n\theta 3) = Hn \quad \text{...(6)}$$

The third and fifth harmonic frequency is eliminated by equaling H3=0, H5=0, and then H1=V1, which represents the fundamental component of the multilevel inverter, so that these equations (3,4,5) are solved by iterative method (Newton-Raphson method); then a sets of switching angles have been achieved as shown in Table 2. [12].

Multilevel inverters can be controlled at low switching frequency is very preferable when the power levels are high and to implemented this, the Selective Harmonic Elimination (SHE) technique can be used [15].

1.2 Modulation Techniques for MLI

The modulation techniques for MLIs can be categorized into two types, first, high-frequency and second, low-frequency or (fundamental frequency) switching strategies. In the SHE technique, the power switches' switching angles in the MLI circuit are initially determined and calculated and then well defined to get rid of the low harmonic orders (3rd, 5th, 7th…etc.) that are near to the fundamental frequency [16].

In order to exclude specific harmonic orders, a bunch of transcendental equations shall be get solved. Some algorithms examples that were used to solve transcendental equations are: Newton–Raphson (NR), genetic algorithms (GA), particle swarm optimization (PSO), and evolutionary programming (EP). It has been discovered that an MLI circuit can effectively use the SHE modulation technique. Due to its ability to decrease power switching losses, this technique is more preferable than others [17].

Many Kinds of digital signal controllers are utilized for the generation of modulating signals for MLCs, such as the PIC16F87XA Microcontroller, Digital Signal Processor (DSP) TMS320LF2407 controller [17], Complex Programmable Logic Device (CPLD) , Arduino [2] and Field Programmable Gate Array (FPGA) [3][15][20], In addition to that the Spartan-3 FPGA is perfectly suited among all kinds of electronics boards due to many features: Flexibility and Programming, Parallel Processing, Hardware Acceleration, high efficiency, simplicity, low latency, customizability and adaptability the FPGA is recommended and used in this work [19]. Xilinx 14.7 Software environment was employed for programming the proposed VHDL code to generate the required signals.

2. SIMULATION RESULTS

The seven multilevel Inverter circuit has been designed and simulated with MATLAB/Simulink software package, as shown in Fig. 4. The output voltage of the seven-level cascaded H-bridge MLI that achieved from the simulation result is shown in Fig. 5.

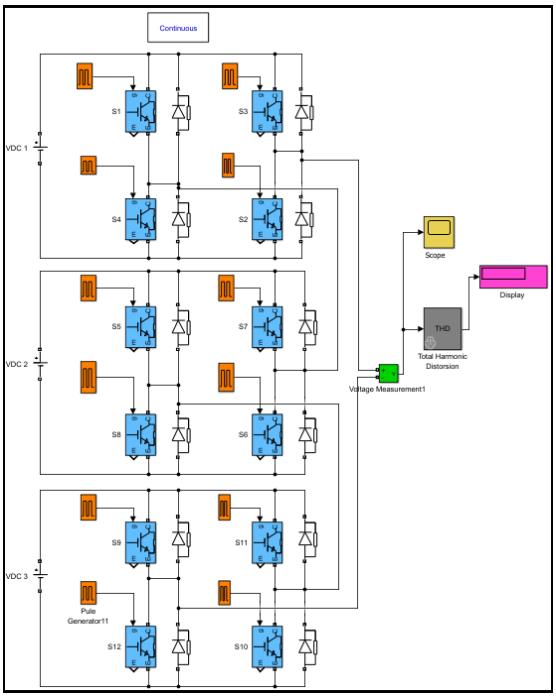


Figure 4. Implemented Simulink model of the seven-level cascaded H-bridge MLI

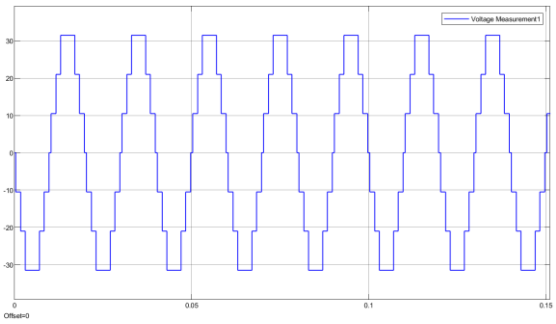


Figure 5. Output voltage waveform of the seven-level cascaded-bridge,MLI

3. Experimental Results

The prototype of the Seven-level CHB inverter was developed in hardware and validated through experimentation, the proposed single-phase inverter was designed using the Power MOSFETs type: IRF3205P211DAJ47 are used as main switches in the H-bridge which can hold up to (55Vdc) the range of the dc power supply was (24Vdc) so as we used three H-Bridges inverters, the upper limit rms value of the multilevel inverter will be around 115VAC.

A gate drive circuit type: TLP250 optocoupler is used to provide isolation between FPGA and the power switches, also the switching pulses signals can be normalized so it can be adequate for

triggering the power switches. The power switches were fired according to the switching angles [14] using the FPGA card. The measuring and testing devices which are used to show the results vales and waveform is (Fluke 190-204 Scope meter, Fluke 435 Power Quality Analyzer, Fluke 345 Power Quality Clamp meter, Fluke 117 True rms Multimeter).

In the below Fig. 6 illustrate the flowchart of the proposed and implemented program in Xilinx ISE Design suite 14.7 software.

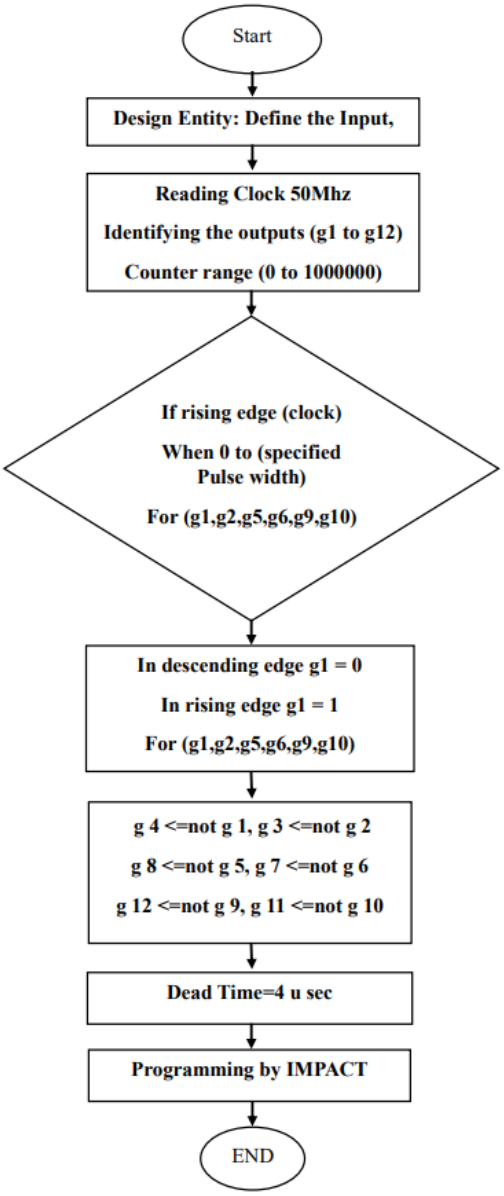


Figure 6. Flowchart of the Implemented VHDL code in Xilinx ISE 14.7

The Flow chart starts with identification of the input and signals,then the FPGA Kit clock (50MHz) with the power switches pulses (signals) will be clarified (g1 to g12),a counter will be used and the required signals durtion will be generated (from 0 to 1000000), the pulses period must be identified in order to generate the signals and their inverse,after that a (4) micro-second was inserted to prevent the ON state for the two power switches on the same leg in each H-Bridge.finally the program is uploading to the FPGA kit via ISE software ,impact function.

In the below Fig. 7 the Experimental setup of the seven-level multilevel inverter with the testing devices.

Figure 7. Experimental Setup of the seven-level multilevel inverter

Also Fig. 8 shows the twelve simulated gate signals for (20msec) time period, the signals are generated by Xilinx ISE 14.7 software.

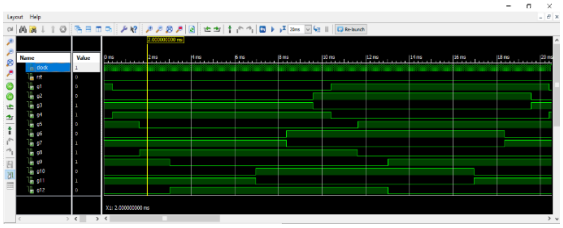
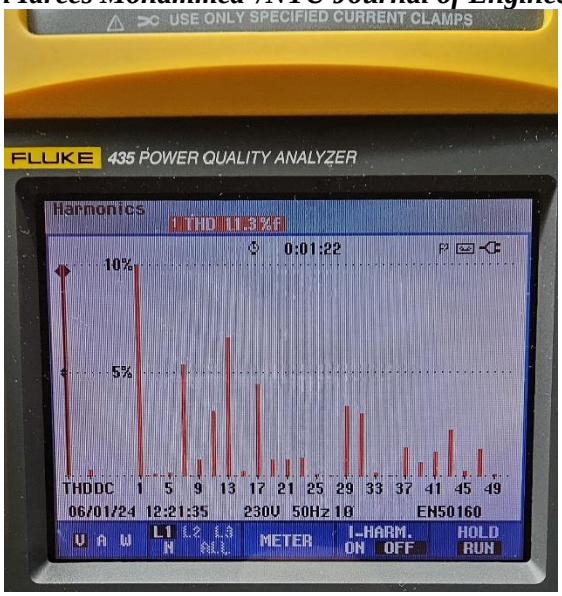
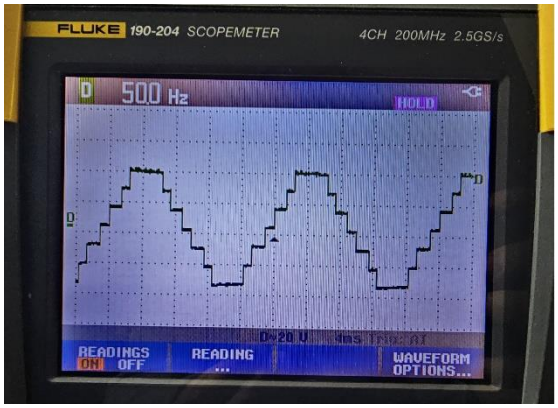


Figure 8. Simulated gate signals (g1-g12) generated from Xilinx ISE 14.7

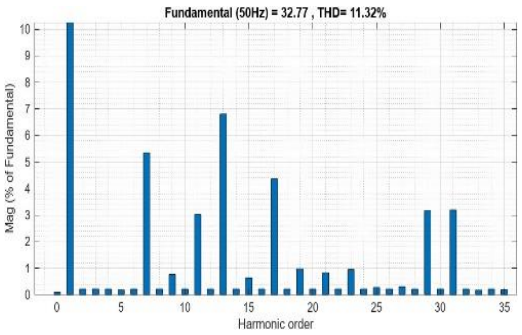
Below in Fig. 9 (a,b,c,d) show the snapshots of the output voltage waveform of the seven-level multilevel inverter, and the spectrum analysis respectively for the (MI=0.75).



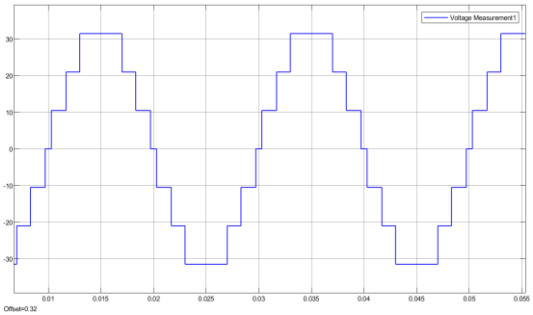
(a) Experimental FFT Analysis



(b) Experimental Output voltage waveform



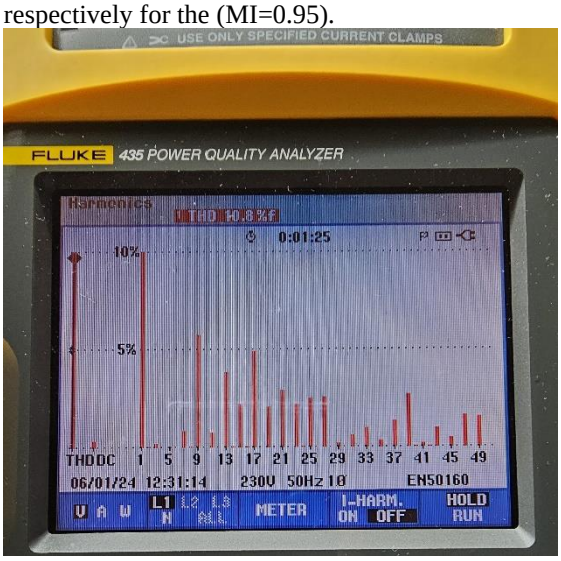
(c) FFT Analysis using MATLAB Simulink



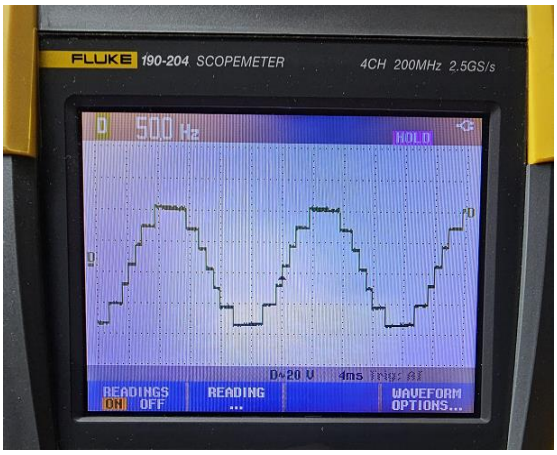
(d) Output voltage waveform using MATLAB Simulink

Figure 9. output voltage waveform and FFT analysis for the 7 level Inverter (MI=0.75)

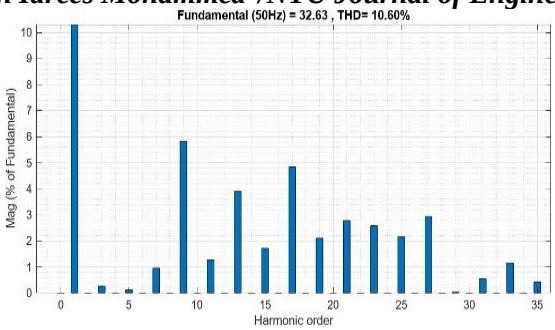
Also in Fig. 10 (a,b,c,d) show the snapshots of the output voltage waveform of the seven-level multilevel inverter, and the spectrum analysis respectively for the (MI=0.95).



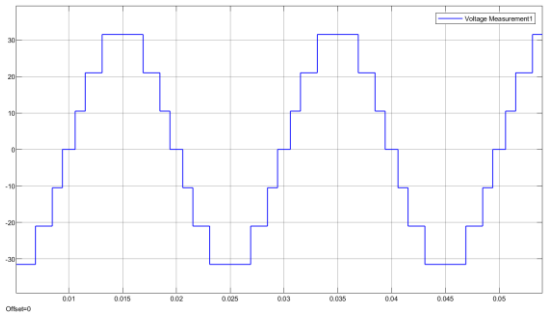
(a) Experimental FFT Analysis



(b) Experimental Output voltage waveform



(c) FFT Analysis using MATLAB Simulink



(d) Output voltage waveform using MATLAB Simulink

Figure 10. output voltage waveform and FFT analysis for the 7 level Inverter (MI=0.90)

The fluctuation of THD with modulation index is seen in Fig. 11 as found in practical and in simulation. The switching angles and THD values for the different modulation indices can be seen in Table 3.

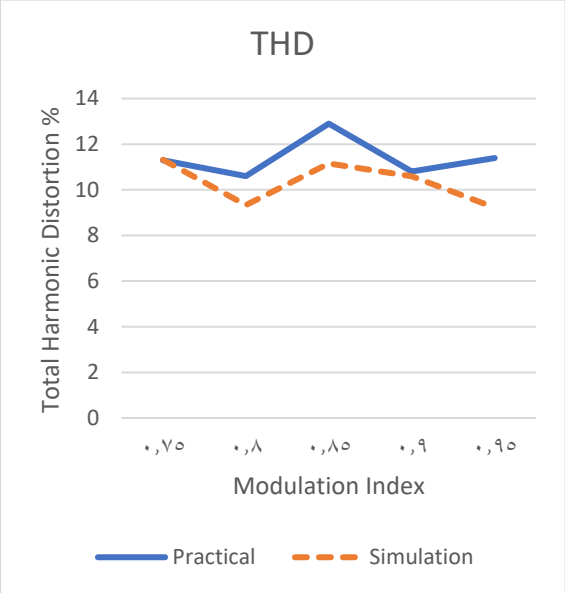


Figure 11. Modulation Index vs Total Harmonic Distortion (Practically and in Simulation)

TABLE 3. Switching angles, Vrms and THD% for seven level multilevel inverter

MI	θ 1	θ 2	θ 3	As in the Paper[2] THD %	Simulated Voltage THD %	Experimental Voltage THD %	V rms
0.75	5.2319	30.4231	53.9134	10.26 %	11.32 %	11.3 %	28.15 V
0.80	7.3593	29.4584	54.4846	9.24 %	9.33 %	10.6 %	27.87 V
0.85	14.3272	25.4782	57.6222	11.13 %	11.16 %	12.9 %	27.49 V
0.90	10.7037	27.5939	55.7440	8.99 %	10.6 %	10.8 %	27.74 V
0.95	8.6268	23.8318	55.0062	9.2 %	9.22 %	11.4 %	28.32 V

4. CONCLUSION

This paper presented the design, implementation, simulatation, and practical comparison of a single-phase seven level multilevel inverter with eliminating the lower order harmonic components by implementing the optimal switching angles that were programmed and generated by ISE software, using VHD language for FPGA Kit.

SHE technique was applied on the CHB inverter,the achieved percentage of the total harmonic distortion THD % has been compared experimentally and also approved by simulation, the results showed a close reproachment between them, As shown in the output voltage waveform spectral analysis in simulation and experimental data, harmonic (3rd and 5th) have been eliminated, while the (7th) harmonic was noticed as the 1st harmonic order.

The results showed apercentage of arround (81%) as the maximum anhancement achieved and that at (MI= 0.8), The best THD% result (10.6%) among all the other values, the Vrms voltage for each case is measured. Future works can be performed to investigate optimum drive switching angles with unequal dc sources and reduced power switches.

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