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Performance Evaluation of a Low Energy Universal Gate for VLSI with 16nm Technology

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Abstract. NAND & NOR logic gates are general purpose logic gates that can be used to build other logic gates.This article describes a new NAND gate based on 3T (3 transistors) which has the correct output logic level and behaves similarly to the previous design NAND gate logic.The proposed structure has faster processing and lower power consumptionwhat makes it ideal for large-scale integration (VLSI) applications. Typical 16nm CMOS fabrication techniques were used for simulation, ,build Nand Gate , and to compare it to Nand Gate with different techniques and design such as using four transistors. It turns out that the amount of delay in this desgin with the selected technology compared to other projects with other technologies is less, that is, 0.02966 ns , which proves that the smaller the delay, the faster the gate operates.

Keywords: Gate, VLSI, NAND , CMOS, delay, logic.

Introduction:

Chip makers are forced to focus on scaling products with faster processing power and longer battery life as demanded for portable devices grows. Power dissipation increased with increasing chip density and complexity. This has a direct impact on battery-powered portable electronic equipment which requires the use of expensive packaging and cooling systems [1]. In a contemporary high-performance CPU, the data channel and memory units consume approximately 45 percent of the total power [1]. The programmerof most data lines and memory modules relies heavily on NAND logic gates. As a result, for the best performance, NAND gates must be precisely designed and analyzed [1].

The Implementation of very low power VLSI applications requires power dissipation by designing low power gated circuits. In fact, digital control systems are designed with NAND or NOR gates and almost all the logic functions required derive from a NAND or NOR continuum.Creating NAND Flash memory requires low power consumption, high reliability, and cost/performance advantages. A complete data storage solution for portable electronic devices [2]. In order to meet the changing demands of current and future applications, the authors have developed the best NAND solutions for these applications [2]. Simulation results were applied to the NAND transistor gate using standard 16nm CMOS output technology showing significant improvement due to shorter transistors with lower power consumption due to count and delay transistors. The details and simulation results of the NAND gate experiment are as follows.

2. Description of Pass Transistor and CMOS Logic

Logical Transistor (PTL) is a popular and widely used alternative to complementary CMOS. As shown in Figure 1, the PTL attempts to reduce the number of transistors required for logic operation by having the main input lead the gate and drain/source connections. This can be seen in Figure 1 [3]. When using as a transistor, the device can carry current in either direction. MOSFET channel N is larger than well-made logic 0, but weak and brittle logic 1 (threshold voltage drop Vth, high logic = VDD-Vthn), while MOSFET P channel exceeds strong logic 1. , Weak logic 0. (Voltage). Dropout threshold) Threshold voltage Vth, low logic = Vthp). Therefore, it can be said that the NFS switch is suitable for the pull-down network & the PMOS switch is suitable for the pull-down network. Upon this background, a quasi-experimental research method has been used in this study [5, 6].

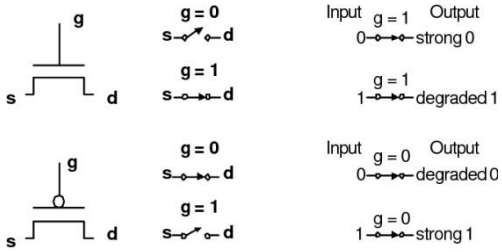

Figure 1: (PTL) Pass- Transistor- Logic.

CMOS transformers are of the most commonly used and supported MOSFETs in design. It works with less energy and also better speed. CMOS inverter Therefore, the noise margin is high, the noise margin is low, and the storage characteristics are good. The CMOS inverter shown in Figure 2 has NOTE and PMOS transistors connected to the sink and gate terminals, the ground connected to the principle of NMOS and the voltage VDD connected to the principle of PMOS, and IN is Connect "G" to exit the gateway cache and "D" to exit. Since logic 1 and logic 0 have different hardware for CMOS, models of PMOS and NMOS provide different output logic 0 and 1.

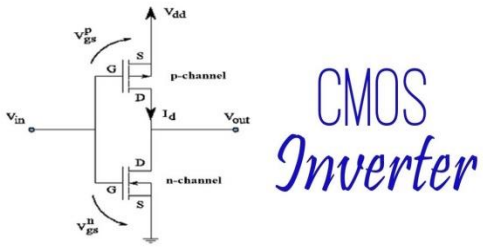

Figure 2: CMOS inverter.

Figure 3 shows the structure of a NAND 3T gate with 3 transistors. The design is based on the logic of the PMOS pass transistor, and the modified CMOS inverters PMOS M1 and NMOS M2 on the left constitute the modified CMOS converter structure. The PMOS M3 acts as a transistor on the right. When A = 1, M3 turns off and the rectifier inverters on the left (M1 and M2) act as standard CMOS inverters. Therefore, input B is output. When A=0 and B=0, M2 is off, M1 and M3 are on, resulting in an undefined "X" output state since M1 pulls the exit node down while M3 pulls the exit node up. Go out.

Similarly, when enabled A = 0 and B = 1, M1, M2 and M3 stopped, resulting in synchronizing the M2 output node, while the m2 synchronizes to increase the output node while synchronizing the output node, while M3 is synchronized to increase the node output. For = 0, b = 0 or 1, we need a strong logical production "1". If the M3 channel display is 6 times a M2 view or view M1, the proposed logical circuit can reach the correct output level. I.E.) WM3 = 6X WM1 = 3X WM2. Thus, the M3M 1 and M2 gets stronger than and the introduction provides strong logic "1" to output at = 0.

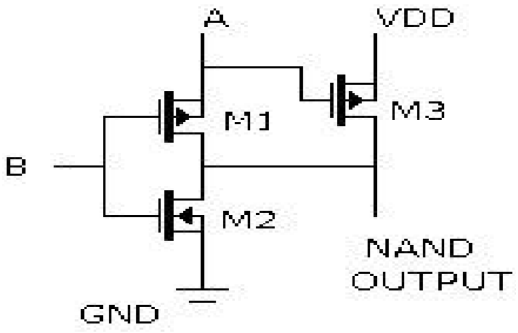

Figure 3: 3T NAND gate.

As shown in Table 1, the full operation of the circuit can be described as a two-input NAND gate. The recommended 3T NAND gate is resistant to body bias due to lack of transistor. Figure 4 illustrates a four-transistor, two-input CMOS NAND gate.

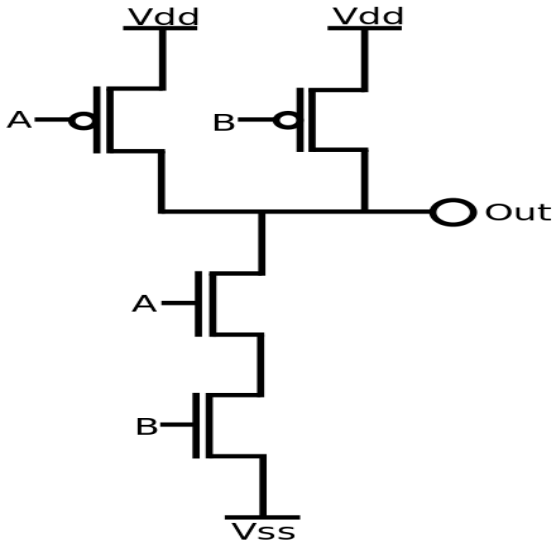

Figure 4: 4T NAND gate

Table 1.three transistor

Input		CMOS INVERTER			NAND(OUTPUT)
A	B	M1	M2	M3	
0	0	on	off	on	1 / VDD
0	1	off	on	on	1 / VDD
1	0	on	off	off	1 / B
1	1	off	on	off	0 / B

The transistor widths W M1 = 48 nm for NMOS M1 , WM3 = 288 nm for PMOS M3 and WM2 = 16 nm for NMOS M2 were used as examples. The length of all transistors should have been L = 16 nm.

3. Simulation and Results

The results of the proposed 3T NAND gate were compared with current NAND gate designs in a series of experiments.Synopsys Custom Designer was used to create all the wiring diagrams for the TSMC 16nm technology. The network list received over time is used to simulate and test performance. The original network list has been modified to work with a process of 16 nm in the technical process of the teacher (BPTM). The modified network list is simulated using SYNOPSYS HSPICE for promotional benefits and latency. All power and delay measurements are performed at the worst temperature of 27 ° C. Circuit performance is measured using area, power dissipation, delay, & the product of power delay.

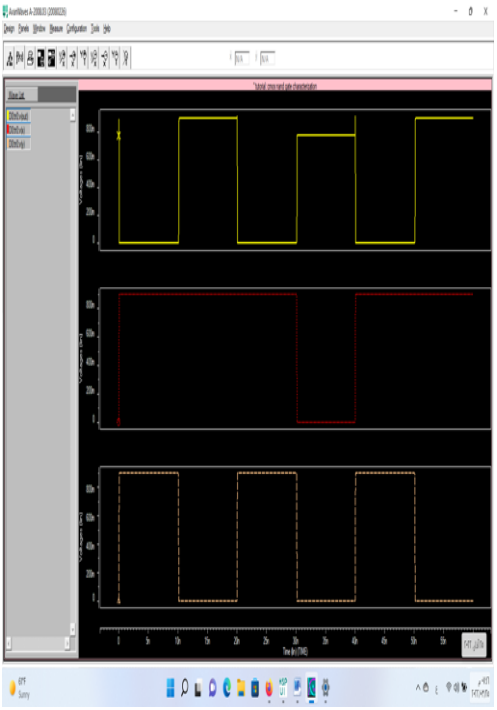

Figure 5: input/output waveforms 3T NAND

Figure 5 shows the input & output waveforms of the proposed 3T NAND gate with a correct logic output level and no voltage drop. Table 2 shows NAND gate circuits with various logic, including CMOS logic [11]. 2-pass transistor logic [4,10], auxiliary transistor logic [8], transistor logic [9]. Gives compare. & dual value logic [7]. Except for the 3T NAND gate, the transistors are WP = 64 nm for PMOS and WN = 32 nm for NMOS, with L = (16 nm). The results in Table 2 are listed below.

Table 2. Comparison of NAND design(CMOS-DPL-CPL-PTL) with 3T NAND gate

	CMOS logic	DPL	CPL	PTL	3t nand
No. of transistor	4	8	8	6	3
Power dissipation(nw)	7.764	8.4314	8.750	7.527	3.2924
Delay(ns)	0.0785	0.0765	0.0761	0.0961	0.02966
Leakage power(nw)	0.800	1.4	1.7	1.02	0.006

Area(um^2)	0.900	1.5	1.8	1.03	0.6

Table 2 illustrate the following conclusion:

- The number of switching transistors increases the dynamic power consumption, power consumption and area.
- Lines 3 and 4 show that there is less power dissipation (dynamic and dispersion) for the 3-transistor NAND gate than for other NAND gate circuits.
- It is possible to get a delay output of a NAND gate based on 3 transistors of three lines, paying special attention to the delay.
- In the implementation area obtained from the project, you can see that the 3 transistor NAND gate, like line 5, needs a smaller area than other circuits.

Table 3. D-latch simulation results using 16nm process technology

d-latch circuit	NO of transistor	Dynamic power(w)	delay	PDP
Using 2T& 3 inverter	10	24.34xE-06	0.303	7.375xE-15
Using 4T &4NAND	12	28.61x E-06	0.386	1.043xE-15
Using 3T &4NAND	12	21.13x E-06	0.139	2.937xE-15

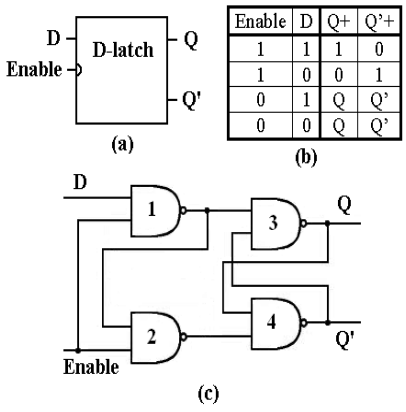

Figure 6: constructed of D –latch

Table 3 shows a comparison of simulation results obtained with the D-latch shown in Figure 6 implemented using 3T NAND gates and other gate designs. With 10 and 12 transistors, the D-latch consumes more power during pulse operation due to the increased number of transmission gates and transistors, respectively. Coupling D-latch using the proposed 3T NAND gates has less internal capacity and less power dissipation by reducing the number of transistors.

4. Conclusion

Finally, the features of 3T NAND gates based on PTL and CMOS logic are introduced. The proposed 3T NAND gate consumes less power and is faster than the current logic architecture. Based on HSPICE simulation on 16nm CMOS process technology at room temperature and under certain conditions. The proposed 3T NAND gate exhibits 23.1% lower power consumption compared to the conventional CMOS(4T) NAND gate. Devices with 3T NAND ports provide ultra-low power consumption to extend battery life. In addition to their current research, the researchers plan to study 3- and 4-input NAND gates with a small number of transistors.

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